Precise Time-of-Flight Measurements Using a Novel High-Resolution Time-to-Digital Converter Architecture

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***Abstract*—Time-to-Digital Converters (TDCs) are widely used for precise time-of-flight (ToF) measurements. The proposed TDC architecture is able to provide very high precision without averaging. As a hardware proof-of-concept, this TDC has been implemented in a 0.35 µm CMOS process and a low-cost FPGA allowing ToF capture at a high repetitive rate to further confirm and evaluate the advantages of our proposed TDC architecture. Most of the measurements are perfectly in accordance with our theoretical claims. This work highlights the advantages of this new TDC in terms of measurement accuracy, calibration, low cost, on-the-fly measurements, and simplicity of implementation. Therefore, it is highly suitable for a ToF architecture.**

***Index Terms*—Time-to-digital converter, self-timed ring oscillator, time resolution, time-of-flight, FPGA, ASIC 0.35 µm CMOS, time measurement.**

I. Introduction

Time-of-Flight (ToF) measurement is the time taken by a signal or particle to propagate between the ToF sensor and an object. ToF measurements are useful in many application fields requiring resolution with picosecond accuracy. It is employed in many applications ranging from medical imaging techniques such as positron emission tomography (PET) to systems for object detection such as radar and lidar systems [1]–[4].

Time-to-Digital Converters (TDCs) are widely used for these precise ToF measurements. The TDC quantifies the measured time interval T, provided by the ToF system, and provides a digital value which often represents the number of time step of a digital clock or a gate delay. For instance, a single-chip receiver architecture for pulsed laser dedicated for 3D imaging applications has been proposed in [4]. In this architecture, 257 TDCs are implemented in connection with a single-photon avalanche diode (SPAD) array. The presented results claim that the characteristics of the receiver are mainly related to the performance of the implemented TDCs. In fact, TDCs are crucial for accurately measuring the time-of flight of the photons.

TDCs are implemented as application-specific integrated circuits (ASIC) or field programmable gate arrays (FPGA). Most of TDCs are implemented as ASIC in order to benefit from the high advances of CMOS technologies and to reach fine grain resolutions [5]–[12]. However, ASIC devices present a long development cycle. In addition, they are expensive, especially for small productions and dedicated products. Conversely, the FPGA-based TDCs benefit from lower cost due to its short development cycle, and present a good flexibility for further improvements, reconfigurations or verification. Additionally, to the implemented TDCs, many other digital blocks can be included in the chip to perform more complex applications. They are frequently used because they offer a good trade-off between ASIC and processor-based systems.

In the simplest TDC architectures, the time resolution is bounded by the gate delay. In order to overcome this technological limitation, sub-gate delay resolution solutions have been proposed [5]–[11]. Moreover, in many applications, a large measurement range is also needed. Therefore, specific architectures have been proposed such as interpolation schemes or multi-quantization levels to achieve wide measurement ranges while ensuring an accurate time resolutions [12]. Nevertheless, while many TDC architectures in the literature can achieve high precision, they often require repetitive measurements. Therefore, on-the-fly measurement for fast non-periodic signals (a few tens of picoseconds) is extremely challenging in TDC designs.

The proposed TDC in this paper is able to provide a very high resolution without averaging. Indeed, it virtually achieves a time resolution as fine as desired by simply increasing the number of stages of a Self-Timed Ring Oscillator (STRO). In fact, a STRO is a multi-phase oscillator, which is able to provide one phase per stage output by propagating several transitions in the ring. The TDC exploits these different STRO phases, which are evenly-spaced thanks to unique analog properties. Thus, a regular time base can be extracted from this STRO and applied for time measurement [13]–[17]. As a hardware proof-of-concept, an ASIC prototype has been designed, fabricated and tested for validating this new class of TDC using 0.35 µm CMOS process [18]. The proposed TDC architecture has also been adapted to be implemented in an Intel Cyclone IV FPGA. This paper demonstrates the advantages of such a TDC in terms of precision, calibration, low-cost and for on-the-fly measurements.

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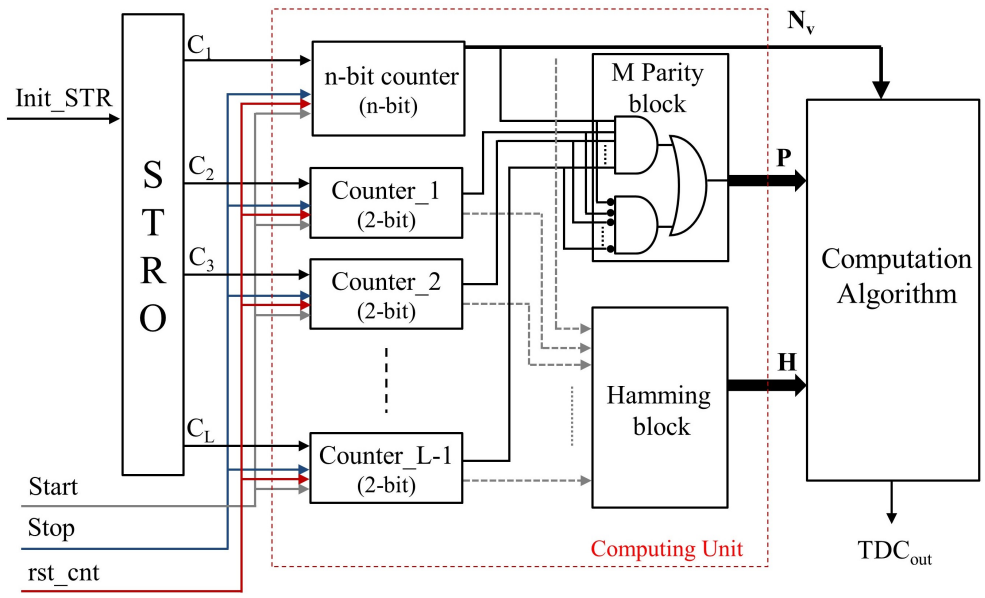

Figure 1. Proposed TDC architecture using an L-stage STRO.

The paper is organized as follows. The proposed TDC architecture based on self-timed ring oscillator is presented in Section II. Section III reports the measurements results based on 0.35 µm CMOS process implementation and the FPGA implementation in Intel Cyclone IV. Finally, Section IV states the paper conclusions.

II. The Proposed TDC Architecture

The proposed STRO-based TDC architecture is presented in Fig. 1. A self-timed ring oscillator (STRO) is a looped control circuit of micropipeline as proposed by [19]. In the STRO several events can propagate concurrently without colliding thanks to a request/acknowledgement handshake protocol. The number of events is set at the ring initialization, and stays invariant. Each STRO stage is composed by a C-element (Muller gate) and an inverter.

Fig. 2 presents the global L-stage STRO architecture. Each stage has two inputs, one (F_i) is forwarded from the output of the previous stage (C_{i-1}) and the other one (R_i) is connected to the output of the next stage (C_{i+1}). The oscillator is modeled with a token game [13]. The stage contains a token if its output is different from the output of the next stage and contains a bubble otherwise. The token propagates to the next stage, if the latter contains a bubble. Oppositely, the bubble replaces this token. The events in the STRO correspond to the token or bubble are set at the ring initialization [13]–[17]. The frequency oscillation of the STRO does not directly depend on the number of stages, but rather on the occupancy ratio which is the number of events N over the number of stages L. In fact, a same frequency can be obtained for different STROs with different number of stages by respecting the same occupancy ratio. Moreover, the ring exhibits a unique

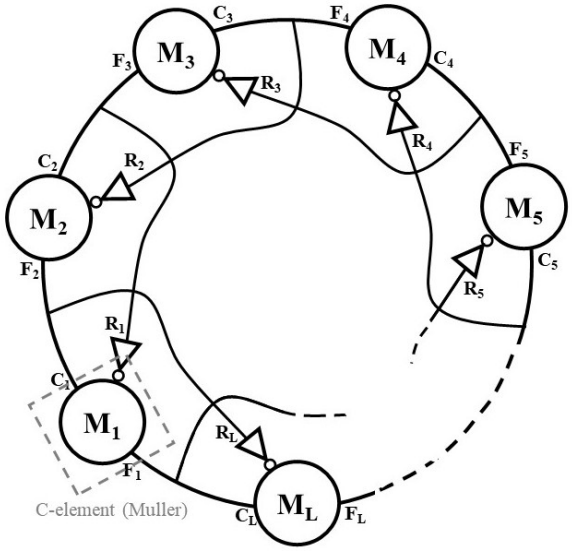

Figure 2. STRO Architecture of L-stages

oscillation mode in which events propagate in the ring with a uniform time spacing (evenly-spaced oscillation mode) [20] due to an analog effect, namely the Charlie's effect [21]. The STRO can provide uniformly distributed events with a sub-gate time resolution $\Delta\varphi = T_{\mathrm{STR}}/2L$. These features have been exploited to propose a new TDC architecture based on STRO which primarily benefits from the uniform distribution of phases.

An L-stage STRO, with a co-prime number of events with L, provides L signals evenly distributed over its half oscillation

period T_{STR}. As a result, the time interval T, generated by Start and Stop signals, can be expressed as a function of $\Delta\varphi$ and T_{STR}. The principle of this structure is to firstly count the number of $T_{\mathrm{STR}}/2$ steps and then to quantify the remaining time with a resolution of $\Delta\varphi$. The equation (1) gives the measured time value T_m.

$$T_m = M \cdot \frac{T_{\mathrm{STR}}}{2} + k \cdot \Delta\varphi = (M \cdot L + k) \cdot \Delta\varphi \qquad (1)$$

A simple architecture derived from this equation is made by a double-edge counter at each STRO output. Basically, k counters show the value $M+1$ while the other $L-k$ counters exhibit the value M.

Obviously, the information about the number of counters showing M or $M+1$ can be derived from the two least significant bits of all counters. Therefore, the architecture can be optimized by using one n-bit counter, which shows the value N_v (for instance, a 5-bit counter), and 2-bit counters for the other outputs. The obtained results from these counters are sufficient to determine M and k as detailed in [16]. The Hamming block (see Fig. 1) uses the LSBs to compute the hamming weight H, which is equal to k when M is even and $L-k$ when M is odd. Then, the Parity block evaluates the parity of M by using the second lower bits of the counters.

The TDC output is given by a data processing algorithm based on the collected data from the n-bit counter, Hamming, and Parity blocks. The time interval T (between the Start and Stop signals) is generated by the finite state machine (FSM).

III. Measurements Results

As a hardware proof-of-concept, an ASIC prototype has been designed, fabricated and tested for validating this new class of TDC using 0.35 µm CMOS process [18]. This proposed TDC architecture has also been adapted to be implemented in an Intel Cyclone IV FPGA.

A. ASIC $0.35\,\mu$m CMOS Measurements

In order to to cover several time resolution with the ASIC test chip, TDCs with different numbers of stages ($L = 9$, $L = 23$, and $L = 61$) have been implemented. According to the selected TDC, the measurement results are sent to the shared outputs of the chip.

The first TDC of 9 stages (with an initialization of 4 tokens) shows an estimated time resolution of 74 ps. This latter is enough larger than the jitter standard deviation of the STRO, which is estimated to be between the 10 ps and 15 ps. A large number of measurements have been made in order to characterize single-shot measurements. Thus, many hits of a calibrated pulse have been carried out and analyzed in order to characterize the TDC performances. The TDC shows a mean value of 2.988 ns with a standard deviation of $\sigma = 1.71$ LSB for an input time $T = 2.95$ ns representing an error of 38 ps. A theoretical time resolution of 72.5 ps is obtained. When the input time is set to $T = 12.5$ ns, the measurement error is 204 ps for a mean value of 12.704 ns and a standard deviation of $\sigma = 2.23$ LSB.

On the other hand, the same measurements from the 23-stage STRO-based TDC have been processed. This TDC was adopted to enhance the time resolution around the jitter variations including 12 tokens. The achieved time resolutions is 29.6 ps. This TDC shows a measurement error of 30 ps for $T = 2.95$ ns (resp. 45 ps for $T = 12.5$ ns), with a mean value of 2.98 ns (resp. 12.545 ns), and a standard deviation of $\sigma = 2.12$ LSB (resp. $\sigma = 2.61$ LSB).

The time resolution of the 61-stage STRO-based TDC initialized with 30 tokens is equivalent to $\Delta\varphi = 13.9$ ps. The resolution of this TDC is about the jitter level. The time measurement of the first hit shows a mean value of 2.93 ns with an error of 20 ps and $\sigma = 2.41$ LSB. However, the measurement of $T = 12.5$ ns presents an important quantification error of 164.0 ps regarding the time resolution of 13.9 ps (the mean value is 12.336 ns). The measurements are highly affected by the jitter, which is obvious with the higher standard deviation (noise $\sigma = 3.69$ LSB).

B. FPGA Implementation

As hardware proof-of-concept, several L-stage STRO-based TDCs configuration ($L = 9, 23, 31, 32, 61, 141$) have been implemented in a low cost EP4CE115F29C7 Intel Cyclone IV FPGA. Each STRO stage is implemented on a single LAB with its corresponding counter. A theoretical time resolution from 317 ps (for 9-stage STRO) to 20 ps (using 141-stage STRO) have been achieved. All implemented TDCs have been characterized for many input time values. The implementation is straightforward. Measurement results point out the advantage of this TDC in terms of measurement accuracy.

For example, a theoretical time resolution of 108.7 ps is obtained with a frequency of 200.0 MHz ($T_{\mathrm{STR}} = 5.0$ ns) thanks to a 23-stage STRO-based TDC. Repetitive measurements for a time value of 9.5 ns and 13 ns have been done in order to characterize the TDC output. 300 measurements have been collected for each time value. The measured time interval reveals that more than 75% (resp. 70%) of the measurements are correct ($\|Err\| \leq 2\Delta\varphi$) and the mean value is around 9.59 ns (resp. 12.94 ns) in the case of $T = 9.5$ ns (resp. $T = 13.0$ ns).

IV. Conclusions

A STRO-based TDC with sub-gate delay time-resolution has been proposed and implemented in 0.35 µm CMOS process and low-cost FPGA as a hardware proof-of-concept allowing us to further evaluate the performance and confirm the advantages of the proposed approach. Most of the measurements are perfectly in accordance with our theoretical claims. They prove the ability of the proposed TDC architecture to enhance the time resolution by simply increasing the number of stages. These results can be further improved by adding a calibration method. Furthermore, higher performances can be enhanced with recent and faster FPGA boards, making it very suitable for time-of-flight measurement applications. In addition, it can easily be duplicated in such a board for ToF architectures.

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